# PRODUCT/PROCESS CHANGE NOTIFICATION

**SUBJECT**

**VNB35N07xx, VNB20N07xx (VN19, VN29): Double Bonding Introduction (2x10mils Al wire)**

**IMPACTED PRODUCTS**

Below VIPower products housed in D2PAK package

| Line | Commercial Product |
|---|---|
| VN19 | VNB35N07-E |
| VN19 | VNB35N07TR-E |
| VN29 | VNB20N07-E |
| VN29 | VNB20N07TR-E |

**MANUFACTURING STEP**

Assembly

**INVOLVED PLANT**

ST Shenzhen (China)

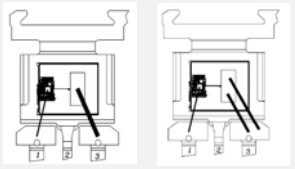
**CHANGE REASON**

Manufacturing Flexibility. Material standardization (wires)

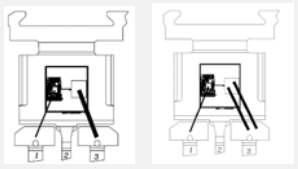
**CHANGE DESCRIPTION**

In order to standardize the assembly processes, on VNB35N07xx and VNB205N07xx will be implemented the doubling wire bonding on source pad, replacing the single 15 mils aluminum wire with double 10 mils aluminum wire.

Current New



VNB35N07



VNB20N07

ZVEI classification
SEM-PA-08

| | |
|---|---|
| **TRACEABILITY** | Dedicated Finished Goods Codes |
| **VALIDATION** | Validation results enclosed in this communication<br>11903 Validation.pdf |
| **SAMPLES** | Available on demand |
| **IMPLEMENTATION** | We are ready to implement the change upon Customer agreement |

# Shenzhen TO263 (D2PAK)
# VN19-VN29 doubling aluminum wire

# Outline

# Change description

- The purpose of this document is to report the qualification activity performed on the two silicon lines VN19 and VN29 assembled in TO263 (D2PAK) package at ST Shenzhen plant (China). The qualification evidences reported hereafter are related to the replacement of the 15mils aluminum wire on Source pad with two 10mils aluminum wires.
- Compared with all the VIPower® products assembled in TO263(D2PAK), the VN19 and VN29 are the only 2 using the 15mils aluminum wire, so the change is proposed in order to standardize the wire material and to improve the line efficiency. Moreover the usage of 10mils wire needs less ultrasonic power during wire bonding operation and that will reduce the mechanical stress to the bonding pad.
- This report shows the positive results achieved by the usage of the double 10mils aluminum wire on Source pad without changing the current assembly process flow and while ensuring the same quality and electrical characteristics as VN19 and VN29 product lines assembled in TO263(D2PAK) package.

# BOM comparison

| Current Bill of Material | |
|---|---|
| **ITEM** | **MATERIAL** |
| WIRE | WIRE Aluminum D15 |
| WIRE | WIRE Aluminum D5 |
| FRAME | FRAME TO263 |
| PREFORM | PREFORM Pb/Ag/Sn |
| RESIN | RESIN SUMITOMO EME7026 |

| New Bill of Material | |
|---|---|
| **ITEM** | **MATERIAL** |
| WIRE | WIRE Aluminum D10 |
| WIRE | WIRE Aluminum D5 |
| FRAME | FRAME TO263 |
| PREFORM | PREFORM Pb/Ag/Sn |
| RESIN | RESIN SUMITOMO EME7026 |

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# ZVEI guidelines

- According to ZVEI recommendations, the notification is required.

| | | Assessment of impact on Supply Chain regarding following aspects<br>- contractual agreements<br>- technical interface of processability/manufacturability of customer<br>- form, fit, function, quality performance, reliability | Remaining risks on Supply Chain? | | Understanding of semiconductors experts | Examples to explain |
|---|---|---|---|---|---|---|
| | ID | Type of change | No | Yes | | |
| X | SEM-PA-08 | Change of wire bonding | P | P | Material, diameter, change in bonding diagram and / or change in process resulting in a new technology. | e.g. change from Au to Cu material<br>e.g. change from 25µm to 23µm diameter<br>e.g. change from single to double bond<br>e.g. change from stich bond to stich on ball bond. |

**Extract from ZVEI** ZVEI: Die Elektroindustrie

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# Selected Test Vehicle

- VIPower® M0A2 Technology:
  - TO263 (D2PAK) : VNB35N07-E / VNB35N07TR-E (Silicon Line VN19)
  - TO263 (D2PAK) : VNB20N07-E / VNB20N07TR-E (Silicon Line VN29)

# Reliability Evaluation Report
# VNB35N07, VNB20N07 new BOM assessment

| General Information | |
|---|---|
| **Commercial Product :** | VNB35N07, VNB20N07 |
| **Product Line :** | VN19, VN29 |
| **Package :** | D2PAK |
| **Silicon Technology :** | VIPower-M02 |

***Note:*** *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile for Automotive Application. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Revision history

| Rev. | Changes description | Author | Date |
|---|---|---|---|
| A | Initial Release | A. Vilardo | 27/11/2019 |

Approved by

| Function | Location | Name | Date |
|---|---|---|---|
| Division Reliability Manager | ST Catania (Italy) | A. Marmoni | 27/11/2019 |

## TABLE OF CONTENTS

# 1 RELIABILITY EVALUATION OVERVIEW

## 1.1 Objective

Aim of this report is to present the results of the reliability evaluations performed on **VNB35N07** and **VNB20N07** (VN19 and VN29 as ST internal silicon line) to evaluate a wire bonding change on source pad. Because of these are the only two ViPower products assembled in the D2Pak using 15mils wire, the change is proposed in order to standardize the wire material and to improve the line efficiency reducing the equipment set-up.
Moreover the usage of 10mil wire needs less ultrasonic power during wire bonding operation and will reduce the mechanical stress to the bonding pad.

VNB35N07 and VNB20N07 are OMNIFET fully auto-protected Power MOSFET, intended for replacement of standard power MOSFETS in DC to 50 KHz applications.

Both the devices are designed in VIPower M02 technology, assembled in ST Shenzhen (CHINA) in D2PAK package and diffused in ST Catania CT6" (Italy) Wafer fab the VNB35N07 and in ST Singapore SG6" wafer fab the VNB20N07.

## 1.2 Reliability Strategy and Test Plan

### 1.2.1 Reliability strategy

Reliability trials performed as part of this reliability evaluation are in agreement with ST 0061692 and **AEC Q100 rev. H Grade 1** specification and are listed in below Test Plan. For details on test conditions, generic data used and specifications references refer to test results summary in section 3.

### 1.2.2 Test Plan

## AEC-Q100 TEST PLAN

| TEST GROUP | TEST NAME | DESCRIPTION / COMMENTS | TEST FLAG |
|---|---|---|---|
| A<br>Accelerated Environment Stress Tests | PC (JL3) | Preconditioning (JL3+3 reflows simulation) | Yes |
| | THB | Temperature Humidity Bias | Yes |
| | AC | Autoclave at 2atm | Yes |
| | TC | Temperature Cycling | Yes |
| | PTC | Power Temperature Cycling | Not Applicable |
| | HTSL | High Temperature Storage Life | Yes |
| B<br>Accelerated Lifetime Simulation Tests | HTOL | High Temperature Operating Life | Not Applicable |
| | ELFR | Early Life Failure Rate | Not Applicable |
| | EDR | Endurance Data Retention | Not Applicable |
| C<br>Package Assembly Integrity Tests | WBS | Wire Bond Shear | Yes |
| | WBP | Wire Bond Pull | Yes |
| | SD | Solderability | Not Applicable |
| | PD | Physical Dimension | Not Applicable |
| | SBS | Solder Ball Shear | Not Applicable |
| | LI | Lead Integrity | Not Applicable |
| D<br>Die Fabrication Reliability Tests | Test list is reported in section 5 | Performed during process qualification | Not Applicable |
| E<br>Electrical Verification Tests | ESD (HBM) | Electrostatic Discharge (Human Body Model) | Not Applicable |
| | ESD (CDM) | Electrostatic Discharge (Charged Device Model) | Not Applicable |
| | LU | Latch Up | Not Applicable |
| | ED | Electrical distribution | Not Applicable |
| | FG | Fault grading | Not Applicable |
| | CHAR | Characterization | Not Applicable |
| | EMC | Electromagnetic Compatibility | Not Applicable |
| | SC | Short Circuit Characterization | No |
| | SER | Soft Error Rate | Not Applicable |
| | LF | Lead(Pb) Free: (see AEC-Q005) | Not Applicable |
| F<br>Defect Screening Tests | Test list is reported in section 5 | To be implemented starting from first production lot | No |
| G<br>Cavity Package Integrity Tests | Test list is reported in section 5 | N/A: not for plastic packaged devices | Not Applicable |

In the below table a comparison between the AEC-Q100 and ZVEI requirements vs the applied ST qualification plan is reported:

| | Test Group A | | | | | Test Group B | | Test Group C | | | | Test Group D | | | | | Test Group E | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | THB | AC | TC | PTC | HTSL | HTOL | ELFR | WBS | WBP | SD | PD | EM | TDDB | HCI | NBTI | SM | HBM | CDM | LU | ED | EMC | SC |
| AEC-Q100 | x | x | x | * | x | | | x | x | | | | | | | | | | | | | x |
| ZVEI | x | x | x | * | x | | | x | x | | | x | | | | | | | | | | x |
| ST | x | x | x | | x | | | x | x | | | | | | | | | | | | | |

Rationale for ST qualification plan:

- * PTC not applicable, performed only when wire diameter decreases.
- EM test is part of the ZVEI Die Fabrication Reliability Tests and therefore it is to be performed in case of Front End changes
- SC: not performed because considering that was not performed at time of product release in the market, no gap analysis to be done as effect of these changes. More over as per AEC-Q100 this test should be performed per agreement between customer and supplier.

## 1.3 Conclusion

All reliability tests (1x AEC-Q100 requirement) have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

Wire Bond Pull/Shear tests (WBP, WBS) as Package Assembly Integrity (test Group C) performed before and after the package oriented stress test pointed out neither abnormal break loads nor forbidden failure modes. SAM analysis performed after the package oriented stress test, pointed out no delamination at the Die/Molding Compound, Die-Pad/Molding Compound and Die Attach Material interfaces.

**Based on the overall results obtained, replacing 1X 15mil Al wire with 2X 10mil Al wires in VNB35N07, VNB20N07 devices assembled in D2PAK package in SHENZEN , positively passed reliability evaluation performed in agreement to AEC_Q100 Rev.H.**

# 2. Product Characteristics

## 2.1. Generalities

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# VNP35N07-E, VNB35N07-E, VNV35N07-E

OMNIFET: fully autoprotected Power MOSFET

**Datasheet – production data**

TO-220 D2PAK PowerSO-10

## Features

| Type | $V_{clamp}$ | $R_{DS(on)}$ | $I_{lim}$ |
|---|---|---|---|
| VNP35N07-E | 70 V | 0.028 Ω | 35 A |
| VNB35N07-E | 70 V | 0.028 Ω | 35 A |
| VNV35N07-E | 70 V | 0.028 Ω | 35 A |

- Automotive qualified
- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET
- Standard TO-220 package
- Compliant with 2002/95/EC European directive

## Description

The VNP35N07-E, VNB35N07-E and VNV35N07-E are monolithic devices made using STMicroelectronics VIPower® technology, intended for replacement of standard Power MOSFETs in DC to 50 KHz applications.

Built-in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

**Table 1. Device summary**

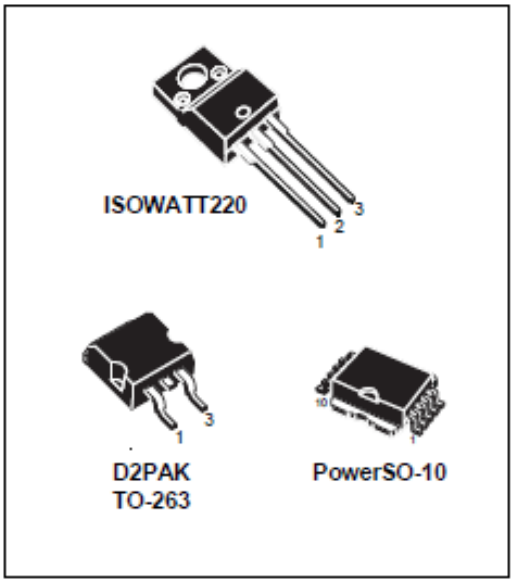
| Package | Order codes | |
|---|---|---|
| | Tube | Tape and reel |
| TO-220 | VNP35N07-E | VNP35N07TR-E |
| $D^2PAK$ | VNB35N07-E | VNB35N07TR-E |
| PowerSO-10 | VNV35N07-E | VNV35N07TR-E |

# VNP20N07FI
# VNB20N07/VNV20N07

## "OMNIFET": FULLY AUTOPROTECTED POWER MOSFET

| TYPE | $V_{clamp}$ | $R_{DS(on)}$ | $I_{lim}$ |
|---|---|---|---|
| VNP20N07FI | 70 V | 0.05 Ω | 20 A |
| VNB20N07 | 70 V | 0.05 Ω | 20 A |
| VNV20N07 | 70 V | 0.05 Ω | 20 A |

- LINEAR CURRENT LIMITATION
- THERMAL SHUT DOWN
- SHORT CIRCUIT PROTECTION
- INTEGRATED CLAMP
- LOW CURRENT DRAWN FROM INPUT PIN
- DIAGNOSTIC FEEDBACK THROUGH INPUT PIN
- ESD PROTECTION
- DIRECT ACCESS TO THE GATE OF THE POWER MOSFET (ANALOG DRIVING)
- COMPATIBLE WITH STANDARD POWER MOSFET

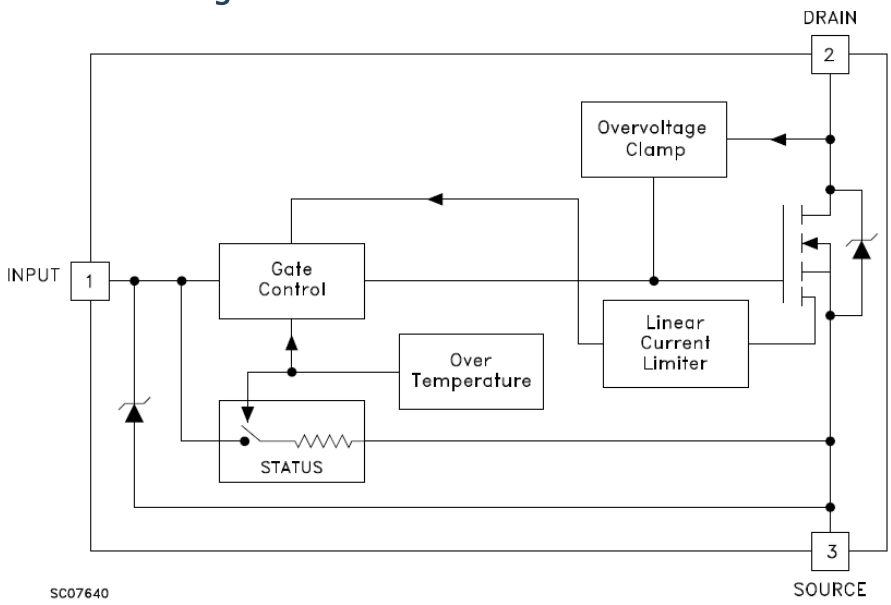



**DESCRIPTION**

The VNP20N07FI, VNB20N07 and VNV20N07 are monolithic devices made using STMicroelectronics VIPower M0 Technology, intended for replacement of standard power MOSFETS in DC to 50 KHz applications. Built-in thermal shut-down, linear current limitation and overvoltage clamp protect the chip in harsh enviroments.

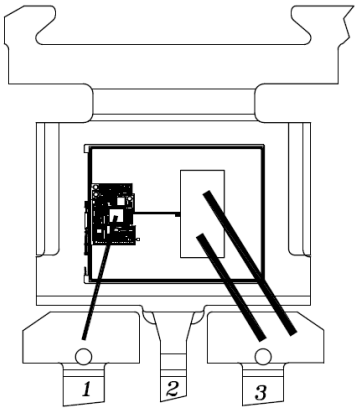
Fault feedback can be detected by monitoring the voltage at the input pin.

## 2.2. Block diagram

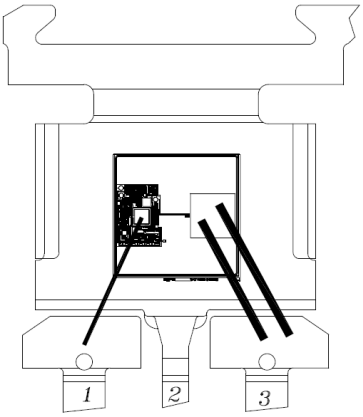


## 2.3. Bonding diagram

VNB35N07




VNB20N07




## 2.4 Traceability

### 2.4.1 Wafer Fab information

| Device | VNB35N07 | VNB20N07 |
|---|---|---|
| Wafer fab name / location | ST Catania CT6 | ST Singapore SG6 |
| Wafer diameter (inches) | 6” | 6” |
| Silicon process technology | VIPower M0A2 | VIPower M0A2 |
| Die finishing front side | SIN | SIN |
| Die finishing back side | Ti-Ni-Au | Ti-Ni-Au |
| Die size (micron) | 4290x5560 | 3870 x 3870 |
| Metal levels/ materials/ thicknesses | 1 /AlSi/ 3.2um | 1 /AlSi/ 3.2um |

### 2.4.2 Assembly information

| Assembly plant name / location | ST SHENZHEN (CHINA) |
|---|---|
| Package descrition | D2PAK |
| Lead frame finishing (material/thickness) | FRAME TO263 Dt 40u Ve5 OptF/G/H SelNiNiP |
| Die attach material | PREFORM Pb/Ag/Sn 95.5/2.5/2 |
| Wire bonding material/diameter | WIRE Al D5, Al D10 |
| Molding compound material | RESIN SUMITOMO EME7026 |
| Package Moisture Sensitivity Level (JEDEC J-STD020D) | MSL3 |

### 2.4.3 Reliability Testing information

| Reliability laboratory location | ST Catania (ITALY), ST Shenzhen (CHINA) |
|---|---|

# 3 TESTS RESULTS SUMMARY

## 3.1 Lot Information

| Lot # | Diffusion Lot | Assy Lot | Note |
|---|---|---|---|
| 1 | 3816866 | GK84018301 | VNB35N07 |
| 2 | 6820KJ7 | GK84017Y01 | VNB20N07 |
| 3 | 6827JPH | GK84018001 | VNB20N07 |
| 4 | 6829F5J | GK8440UQ01 | VNB20N07 Reference Lot |

## 3.2 Tests results summary

Test method revision reference is the one active at the date of reliability trial execution.

**TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS**

| Test | # | Reference | AEC-Q100<br>STM Test Conditions | Lots | S.S. | Total | Results<br>FAIL/SS/Lots | Comments |
|---|---|---|---|---|---|---|---|---|
| PC | A1 | JESD22-A113<br>J-STD-020 | 24h bake@125°C, including 5<br>Temperature Cycling<br>Ta=-40°C/+60°C<br><br>ACC MSL3 (52h@60C/60%RH)<br><br>3x Reflow simulation<br>Peak Reflow Temp= 260°C<br><br>100 Temperature Cycling<br>Ta=-50°C/+150°C | 4 | 231 | 924 | 0/231/4 | |
| THB | A2 | JESD22 A101<br>JESD22 A110 | Ta=85°C, 85%RH,<br>Duration= 1000hrs | 4 | 77 | 308 | 0/77/4 | |
| AC | A3 | JESD22 A102<br>or JESD22<br>A118<br>or JESD22-<br>A101 | **ENV. SEQ.**<br>**Environmental Sequence**<br>TC (Ta=-65°C / +150°C for<br>100 cycles) +<br>AC (Ta=121°C, Pa=2atm for<br>96 hours) | 4 | 77 | 308 | 0/77/4 | |
| TC | A4 | JESD22 A104 | Ta=-55°C /+150 °C<br>Duration= 1000 cycles | 4 | 77 | 308 | 0/77/4 | |
| PTC | A5 | JESD22 A105 | Ta=-40°C /+125 °C<br>Duration=1000 cycles | - | - | - | - | Not Applicable |
| HTSL | A6 | JESD22 A103 | Ta= 150°C<br>Duration= 1000hrs | 4 | 77 | | 0/77/4 | |

## TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS

| Test | # | Reference | AEC-Q100 STM Test Conditions | Lots | S.S. | Total | Results FAIL/SS/Lots | Comments |
|---|---|---|---|---|---|---|---|---|
| HTOL | B1 | JESD22 A108 | TJ=150°C<br>Duration= 1000hrs<br><br>Bias dynamic stress (**OLT**) | – | – | – | – | Not Applicable |
| HTOL | B1 | JESD22 A108 | Ta=150°C<br>Duration= 1000hrs<br><br>Bias static stress (**HTB**) | – | – | – | – | Not Applicable |
| ELFR | B2 | AEC-Q100-008 | Ta max=150°C<br>Duration=24hrs | – | – | – | – | Not Applicable |
| EDR | B3 | AEC-Q100-005 | Specific tests and conditions to be defined in case of NVM | – | – | – | – | Not Applicable |

## TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS

| Test | # | Reference | AEC-Q100 STM Test Conditions | Lots | S.S. | Total | Results FAIL/SS/Lots | Comments |
|---|---|---|---|---|---|---|---|---|
| WBS | C1 | AEC-Q100-001<br>AEC-Q003 | Wire Bond Shear: (Cpk > 1.67) | 4 | min 5 units | min 15 units | All measurement within spec limits | All assembly lots |
| WBP | C2 | Mil-STD-883, Method 2011<br>AEC-Q003 | Wire Bond Pull: (Cpk > 1.67) | 4 | min 5 units | min 15 units | All measurement within spec limits | All assembly lots |
| SD | C3 | JESD22 B102<br>JSTD-002D | Solderability: (>95% coverage) 8hr steam aging prior to testing | – | – | – | – | Not Applicable |
| PD | C4 | JESD22 B100, JESD22 B108<br>AEC-Q003 | Physical Dimensions: (Cpk > 1.67) | – | – | – | – | Not Applicable |
| SBS | C5 | AEC-Q100-010<br>AEC-Q003 | Only for BGA package | – | – | – | – | Not Applicable |
| LI | C6 | JESD22 B105 | Not required for Surface Mount Devices | – | – | – | – | Not Applicable |

## TEST GROUP D – DIE FABRICATION RELIABILITY TESTS

| Test | # | Reference | AEC-Q100 STM Test Conditions | Lots | S.S. | Total | Results FAIL/SS/Lots | Comments |
|---|---|---|---|---|---|---|---|---|
| EM | D1 | JESD61 | Data, test method and criteria available upon request | – | – | – | – | Not Applicable |
| TDDB | D2 | JESD35 | Data, test method and criteria available upon request | – | – | – | – | Not Applicable |
| HCI | D3 | JESD60 & 28 | Data, test method and criteria available upon request | – | – | – | – | Not Applicable |
| NBTI | D4 | JESD90 | Data, test method and criteria available upon request | – | – | – | – | Not Applicable |
| SM | D5 | JESD61, 87, & 202 | Data, test method and criteria available upon request | – | – | – | – | Not Applicable |

## TEST GROUP E – ELECTRICAL VERIFICATION

| Test | # | Reference | AEC-Q100 STM Test Conditions | Lots | S.S. | Total | Results FAIL/SS/Lots | Comments |
|---|---|---|---|---|---|---|---|---|
| TEST | E1 | User/Supplier Specification | Pre and Post Stress Electrical Test | All | All | All | Passed | All parametric and functional tests |
| HBM | E2 | AEC-Q100-002 | Target: ±2kV | – | – | | – | Not Applicable |
| CDM | E3 | AEC-Q100-011 | Target:<br>±750V on corner pins<br>± 500V all others | – | – | | – | Not Applicable |
| LU | E4 | AEC-Q100-004 | Current Injection<br>Class II – Level A (+/– 100mA) | – | – | – | – | Not Applicable |
| ED | E5 | AEC-Q100-009<br>AEC-Q003 | Electrical Distributions: (Test @ Rm/Hot/Cold) (where applicable, Cpk >1.67) | – | – | – | – | Not Applicable |
| EMC | E9 | SAE J1752/3 | Electromagnetic Compatibility (Radiated Emissions) | – | – | – | – | Not Applicable |
| SC | E10 | AEC Q100-012 | Short Circuit Characterization | – | – | – | – | Not Applicable |
| SER | E11 | JESD89-1<br>JESD89-2<br>JESD89-3 | Applicable to devices with memory | – | – | – | – | Not Applicable |
| LF | E12 | AEC-Q005 | Lead(Pb) Free: (see AEC-Q005) | – | – | – | – | Not Applicable |

## TEST GROUP F – DEFECT SCREENING TESTS

| Test | # | Reference | AEC-Q100 STM Test Conditions | Lots | S.S. | Total | Results FAIL/SS/Lots | Comments |
|---|---|---|---|---|---|---|---|---|
| PAT | F1 | AEC-Q001 | Process Average Testing: (see AEC-Q001) | Not performed on qualification lots. It will be implemented starting from first production lot | | | | |
| SBA | F2 | AEC-Q002 | Statistical Bin/Yield Analysis: (see AEC-Q002) | | | | | |

## TEST GROUP G – CAVITY PACKAGE INTEGRITY TESTS

| Test | # | Reference | AEC-Q100 STM Test Conditions | Lots | S.S. | Total | Results FAIL/SS/Lots | Comments |
|---|---|---|---|---|---|---|---|---|
| MS | G1 | JESD22 B104 | Mechanical Shock | Not Applicable: not for plastic packaged devices | | | | |
| VFV | G2 | JESD22 B103 | Variable Frequency Vibration | | | | | |
| CA | G3 | MIL-STD-883 Method 2001 | Constant Acceleration | | | | | |
| GFL | G4 | MIL-STD-883 Method 1014 | Gross and Fine Leak | | | | | |
| DROP | G5 | | Drop Test, Package Drop | | | | | |
| LT | G6 | MIL-STD-883 Method 2004 | Lid Torque | | | | | |
| DS | G7 | MIL-STD-883 Method 2019 | Die Shear | | | | | |
| IWV | G8 | MIL-STD-883 Method 1018 | Internal Water Vapor | | | | | |

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# Conclusions

- The doubling aluminum wire performed on VN19 and VN29 product lines, assembled in TO263(D2PAK) package in ST Shenzhen plant (China) ensures:
  - no change on quality about the current assembly process flow;
  - the same electrical characteristics for the product lines impacted.